UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,049,526 B2
APPLICATION NO. : 10/700209
DATED : May 23, 2006
INVENTOR(S) : Jones et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 7, line 18, should read:

9. A method comprising:

fabricating a first metallization layer comprising a first microvia pad; and

fabricating a second metallization layer comprising a second microvia pad wherein the [a] microvia pad having a base and a projection extending from the base; and

fabricating an intermediate layer disposed between the first metallization layer and the second metallization layer, the intermediate layer comprising a microvia electrically coupled to the first microvia pad and to the second microvia pad wherein the [a] microvia having plurality of surfaces facing a plurality of surfaces of the projection.

Col. 8, line 3, should read:

10. [A] The method according to Claim 9, further comprising:

fabricating an electroless conductor disposed between the microvia and the microvia pad,

wherein the microvia pad and the microvia are composed of an electrolytic conductor.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 8, line 12, should read:

11. [A] The method according to Claim 10, wherein fabricating the microvia pad comprises:

fabricating the base; and

fabricating the projection extending from the base after fabricating the base.

Col. 8, line 15, should read:

12. A system comprising:

an integrated circuit package comprising:

a first metallization layer comprising a first microvia pad;

a second metallization layer comprising a second microvia pad having a projection extending in a direction toward the first microvia pad; and

an intermediate layer disposed between the first metallization layer and the second metallization layer, the intermediate layer comprising a microvia electrically coupled to the first microvia pad and to the second microvia pad; and

a double data rate memory electrically coupled to the integrated circuit package.

Col. 8, line 17, should read:

13. [A] The system according to Claim 12, wherein the microvia includes a plurality of surfaces facing a plurality of surfaces of the projection.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 8, line 20, Add Claims 14 and 15

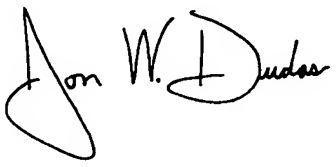
14. [A] The system according to Claim 12, wherein the projection is an integral portion of the second microvia pad.

15. [A] The system according to Claim 12, further comprising:

a motherboard electrically coupled to the integrated circuit package and to the memory.

Signed and Sealed this

Twelfth Day of June, 2007



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